

## CLAIMS

- 1 1. A comparator for an analog-to-digital converter comprising:  
2 - an input for receiving an input signal;  
3 - a bipolar latch stage coupled to the input for performing a latch decision based on said  
4 input signal and for outputting an output signal depending on said decision;  
5 - a reset switch coupled to said bipolar latch stage for resetting said latch stage  
6 subsequent to said latch decision;  
7 - amplification means coupled to the latch stage for amplifying said output signal so that  
8 said amplified output signal is suitable to be input to CMOS circuitry,  
9 wherein said amplification means includes:  
10 - a first tapping or level shift transistor coupled to said bipolar latch stage for,  
11 depending on the latch decision, tapping a collector current from said latch stage,  
12 while leaving the latch decision thereof unaffected, so that a current gain of said bipolar  
13 latch stage can be used to amplify a latch bias current of said bipolar latch stage to  
14 thereby provide for the amplification of said output signal.
- 1 2. The comparator as claimed in claim 1 wherein said input includes a pair of  
2 differential inputs, and wherein said input signal is a differential input signal.
- 1 3. The comparator as claimed in claim 2 wherein said output signal is a differential  
2 output signal, and wherein said amplification means includes a second tapping or level  
3 shift transistor coupled to said bipolar latch stage for, depending on the latch decision,  
4 tapping a collector current from said latch stage, while leaving the latch decision  
5 thereof unaffected, such that a current gain of said bipolar latch stage can be used to  
6 amplify a latch bias current of said bipolar latch stage to thereby provide for the  
7 amplification of said differential output signal.
- 1 4. The comparator as claimed in claim 3 wherein said pair of tapping or level shift  
2 transistors are bipolar transistors.

1 5. The comparator as claimed in claim 3 wherein said bipolar latch stage includes a  
2 pair of bipolar transistors, the base of each of which is coupled to the emitter of a  
3 respective one of said tapping or level shift transistors.

1 6. The comparator as claimed in claim 5 wherein said comparator is adapted to turn  
2 off one of said bipolar latch transistors subsequent to said latch decision to thereby  
3 switch a bias current fed into said one bipolar latch transistor to the base of the other one  
4 of said bipolar latch transistors, whereby a collector current of said other one of said  
5 bipolar latch transistors will be considerably increased.

1 7. The comparator as claimed in claim 3 wherein said comparator is adapted to  
2 directly lead said tapped collector current from said latch stage via one of said tapping  
3 or level shift transistors to one of said differential outputs.

1 8. The comparator as claimed in claim 3 wherein each of said differential outputs  
2 is coupled to an inverter.

1 9. The comparator as claimed in claim 3 wherein said comparator is implemented  
2 in BiCMOS technology.

1 10. The comparator as claimed in claim 3 wherein the bipolar latch stage comprises a  
2 first and a second bipolar transistor arranged in a cross-coupled state, so that  
3 - the collector of the first transistor is connected to the base of the second transistor,  
4 which connection defines a first node; and  
5 - the collector of the second transistor is connected to the base of the first transistor,  
6 which connection defines a second node; and wherein  
7 - the emitters of the first and second transistors are connected to a common electrical  
8 potential.

1 11. The comparator as claimed in claim 10 wherein said pair of differential inputs are  
2 connected, via said input stage, to said first and second nodes, respectively.

1 12. The comparator as claimed in claim 10 wherein  
2 - a first one of said pair of tapping or level shift transistors is connected so that the  
3 emitter thereof is connected to said first node, and the collector thereof is connected, via  
4 a third node, to a first one of said pair of differential outputs; and  
5 - a second one of said pair of tapping or level shift transistors is connected so that the  
6 emitter thereof is connected to said second node, and the collector thereof is connected,  
7 via a fourth node, to a second one of said pair of differential outputs; and wherein  
8 - the bases of said pair of tapping or level shift transistors are connected.

1 13. The comparator as claimed in claim 12 further comprising a bias circuitry for  
2 biasing of the base voltage of said pair of tapping or level shift transistors.

1 14. The comparator as claimed in claim 3 wherein the bipolar latch stage comprises a  
2 first and a second bipolar transistor arranged so that  
3 - the collector of the first transistor is connected to the base of a first one of said pair of  
4 tapping or level shift transistors, which connection defines a first node;  
5 - the collector of the second transistor of the bipolar latch stage is connected to the base  
6 of a second one of said pair of tapping or level shift transistors, which connection defines  
7 a second node;  
8 - the base of the first transistor is connected to the emitter of the second one of said pair  
9 of tapping or level shift transistors;  
10 - the base of the second transistor of the bipolar latch stage is connected to the emitter of  
11 the first one of said pair of tapping or level shift transistors; and  
12 - the emitters of the first and second transistors are connected to a common electrical  
13 potential.

1 15. The comparator as claimed in claim 14 wherein said pair of differential inputs  
2 are, via said input stage, connected to said first and second nodes, respectively.

1 16. The comparator as claimed in claim 14 wherein  
2 - the collector of said first one of said pair of tapping or level shift transistors is  
3 connected, via a third node, to a first one of said pair of differential outputs; and  
4 - the collector of said second one of said pair of tapping or level shift transistors is  
5 connected, via a fourth node, to a second one of said pair of differential outputs.

1 17. The comparator as claimed in claim 1 wherein said bipolar latch stage comprises  
2 four bipolar transistors in a Darlington-coupled state.

1 18. The comparator as claimed in claim 3 wherein  
2 - said bipolar latch stage comprises four bipolar transistors, wherein  
3 - the collector of a first one of said four bipolar transistors is connected to the base of a  
4 second one of said four bipolar transistors, which connection is further connected to the  
5 emitter of a first one of said pair of tapping or level shift transistors;  
6 - the collector of a third one of said four bipolar transistors is connected to the base of a  
7 fourth one of said four bipolar transistors, which connection is further connected to the  
8 emitter of a second one of said pair of tapping or level shift transistors; and  
9 - the collectors of said second and forth ones of said four bipolar transistors are  
10 connected to a voltage supply via an RC circuitry.

1 19. The comparator as claimed in claim 1 further comprising an input stage coupled  
2 to the input for receiving said input signal as a signal suitable for switched capacitor  
3 circuits.

1 20. The comparator as claimed in claim 19 wherein said input stage is adapted to  
2 supply said latch stage with bias current.

- 1 21. The comparator as claimed in claim 1 further comprising a clock for controlling  
2 said reset switch.

- 1    22.    An analog-to-digital converter comprising a plurality of comparators wherein  
2    each comparator comprises:  
3    - an input for receiving an input signal;  
4    - a bipolar latch stage coupled to the input for performing a latch decision based on said  
5    input signal and for outputting an output signal depending on said decision;  
6    - a reset switch coupled to said bipolar latch stage for resetting said latch stage  
7    subsequent to said latch decision;  
8    - amplification means coupled to the latch stage for amplifying said output signal so that  
9    said amplified output signal is suitable to be input to CMOS circuitry,  
10    wherein said amplification means includes:  
11    - a first tapping or level shift transistor coupled to said bipolar latch stage for,  
12    depending on the latch decision, tapping a collector current from said latch stage,  
13    while leaving the latch decision thereof unaffected, so that a current gain of said bipolar  
14    latch stage can be used to amplify a latch bias current of said bipolar latch stage to  
15    thereby provide for the amplification of said output signal.

1 23. A method of operating a comparator for an analog-to-digital converter  
2 comprising the steps of:  
3 - feeding an input signal to an input;  
4 - performing a latch decision based on said input signal and outputting an output signal  
5 depending on said decision by means of a bipolar latch stage coupled to the input;  
6 - resetting said latch stage subsequent to said latch decision by means of a reset switch  
7 coupled to said bipolar latch stage;  
8 - amplifying said output signal, so that said amplified output signal is suitable to be input  
9 to CMOS circuitry; and  
10 - outputting said output signal suitable to be input to CMOS circuitry,  
11 said method being further comprising the steps of:  
12 - depending on said latch decision tapping a collector current from said latch stage,  
13 while leaving the latch decision thereof unaffected, by means of a tapping or level shift  
14 transistor coupled to said bipolar latch stage; and  
15 - using a current gain of said bipolar latch stage to amplify a latch bias current of said  
16 bipolar latch stage to thereby provide for the amplification of said output signal.

1 24. The method as claimed in claim 23 wherein said fed input signal is a differential  
2 input signal and said input includes a pair of differential inputs.

1 25. The method as claimed in claim 24 wherein said output signal is a differential  
2 output signal, and wherein, depending on said latch decision, a collector current is  
3 tapped from said latch stage by means of a second tapping or level shift transistor  
4 coupled to said bipolar latch stage, while leaving the latch decision thereof unaffected,  
5 so that a current gain of said bipolar latch stage can be used to amplify a latch bias  
6 current of said bipolar latch stage to thereby provide for the amplification of said  
7 differential output signal.

1    26.    The method as claimed in claim 25 wherein  
2    - said bipolar latch stage includes a pair of bipolar transistors; and wherein  
3    - one of said bipolar latch transistors is turned off subsequent to said latch decision to  
4    thereby switch a bias current fed into said one bipolar latch transistor to the base of the  
5    other one of said bipolar latch transistors, whereby a collector current of said other one of  
6    said bipolar latch transistors will be considerably increased.

1    27.    The method as claimed in claim 26 wherein said considerably increased collector  
2    current is directly lead from said other one of said bipolar latch transistors via one of  
3    said tapping or level shift transistors to one of said differential outputs.



- 1 28. A method of operating an analog-to-digital converter comprising the step of  
2 operating a plurality of comparators, wherein the operation of each comparator  
3 comprises the steps of:
- 4 - feeding an input signal to an input;
  - 5 - performing a latch decision based on said input signal and outputting an output signal  
6 depending on said decision by means of a bipolar latch stage coupled to the input;
  - 7 - resetting said latch stage subsequent to said latch decision by means of a reset switch  
8 coupled to said bipolar latch stage;
  - 9 - amplifying said output signal, so that said amplified output signal is suitable to be input  
10 to CMOS circuitry; and
  - 11 - outputting said output signal suitable to be input to CMOS circuitry,
- 12 said method being further comprising the steps of:
- 13 - depending on said latch decision tapping a collector current from said latch stage,  
14 while leaving the latch decision thereof unaffected, by means of a tapping or level shift  
15 transistor coupled to said bipolar latch stage; and
  - 16 - using a current gain of said bipolar latch stage to amplify a latch bias current of said  
17 bipolar latch stage to thereby provide for the amplification of said output signal.